

A 915 MHz Active Inductor-Based Band-pass Filter for sub-GHz RF Receivers

Raul P. de Oliveira
Federal University of Pampa
Alegrete, Brazil

rauloliveira.aluno@unipampa.edu.br

Tailize C. De-Oliveira
Federal University of Pampa
Alegrete, Brazil

tailizeoliveira.aluno@unipampa.edu.br

Alessandro G. Girardi
Federal University of Pampa
Alegrete, Brazil

alessandogirardi@unipampa.edu.br

Paulo C. C. de Aguirre
Federal University of Pampa
Alegrete, Brazil
pauloaguirre@unipampa.edu.br

Lucas Compassi-Severo
Federal University of Pampa
Alegrete, Brazil
lucassevero@unipampa.edu.br

Abstract—The implementation of RF integrated circuits at sub-GHz presents some challenges in the use of planar inductors due to their large silicon area and reduced quality factor. To overcome this issue this paper analyzes the implementation of an RLC band-pass filter (BPF) using active inductors (AIs) instead of the planar ones. The preliminary results of the AI implemented in a CMOS 65nm presented an inductance of 7.11 nH, a quality factor of 14.44 and an SRF of 1.23 GHz. The implemented BPF presented a center frequency of 915 MHz with an insertion loss of 13.75 dB and a bandwidth of 680 MHz. The power consumed by the complete circuit was 1.3 mW at 1.2 V.

Index Terms—component, formatting, style, styling, insert

I. INTRODUCTION

The CMOS technology evolution has allowed the fabrication of digital and analog circuits in single-chip. Its characteristic together with the high-integration capability makes possible the design of complex systems from digital processors to RF transceivers. The digital part takes advantage of channel length reduction to increase the transistor density and improves the circuit capacity. On the other hand, the analog and RF circuits are very dependent on the passive devices, such as capacitors and inductors that are not completely scaled down.

Integrated inductors are necessary for almost all RF circuit implementations since the resonance phenomenon should be employed to tune the circuits. The main drawback of the magnetic components is their size which represents an important slice of the IC silicon area. Additionally, it should be designed using electromagnetic tools and are very sensitive to substrate losses and circuit proximity.

At sub-GHz frequency, it is very challenging to design integrated inductors due to their increased size and reduced quality factor (Q). At these frequency bands, such as the 915 MHz ISM, are several applications that required RF integrated circuits (RFIC), such as RF-ID tags and readers, internet of Things (IoT) devices and long-range communication (LoRa). The simplified block of a typical RF front-end is shown in Fig. 1. It is composed of a low-noise amplifier (LNA), a band-pass filter (BPF), a mixer, and a local oscillator (LO) [5]. In turn, the bandpass filter is responsible for reducing the

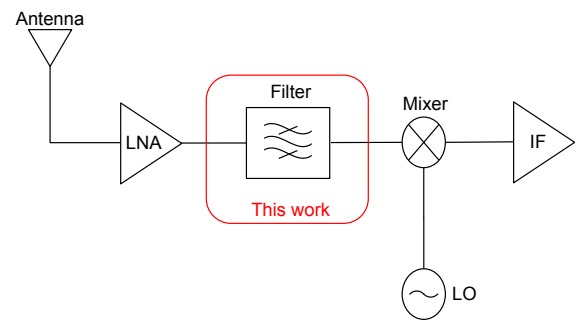


Fig. 1. Simplified block diagram of a typical RF receiver front-end.

implementation complexity of the local oscillator, through the central passing frequency.

An alternative to overcome the issue of using passive inductors is the use of active inductors (AI) that emulated the electrical behavior of magnetic elements using CMOS transistors. The AIs in general occupy less area than the passive inductors and can operate in a wide range of frequencies, being able to tune without interruption covering process and temperature variations [6]. Additionally, according to its biasing point, it can be implemented as a tunable device.

The implementation of active inductors originates from the theory of gyrator. This theory is defined by two transconductors connected in positive and negative inputs, making a back-to-back connection between both transconductors, however, when the capacitance is connected to the output of the circuit, this topology is called by gyrator-C as shown in Fig. 2. The kind of these circuits can be able to generate a variable inductance on the input node according to the transconductances of both transconductors given by $L = C/g_{m1}g_{m2}$ [3].

The BPF proposed is designed using a tuned L-C network composed of an active inductor and a capacitor in parallel connection. From the theory of L-C circuits, the resonance frequency, when in this case is the same as the passing frequency is given by the ratio $f = 1/2\pi\sqrt{LC}$ [1].

This paper presents the preliminary results of the design

of an AI-based bandpass filter intended to be used in RF receivers. This circuit was designed in a CMOS 65 nm process to work with 1.2 V at 915 MHz.

This paper is organized as follows: Section II presents the proposed active inductor, Section III presents the bandpass filter methodology and, finally, Section IV concludes this work and proposes future works.

II. PROPOSED ACTIVE INDUCTOR

The proposed active inductor is based on a basic gyrator-C topology, as shown in Fig. 2. The implementation of transconductors 1 and 2 are based on a common-source and a source-follower amplifier, respectively. Fig. 4 the implemented circuit [7] in which transistors M_1 and M_2 generate the transconductances g_{m1} and g_{m2} and transistors M_3 and M_4 work as current sources to bias the transconductors. The bias voltages v_{bias_1} and v_{bias_2} are provided by biasing current-mirrors.

Fig. 2 shows the small-signal model of the AI circuit of Fig. 4. By circuit analysis, the equivalent input impedance (Z_{in}) can be evaluated at node V_2 , as given by Equation (1).

$$Z_{in}(s) = \frac{sC_D + A}{s^2C_D C_X + s(C_X A + C_D B) + AB + g_m} \quad (1)$$

here the C_D and C_X parameters model the parasitic capacitances of each transistor, and also the coefficients A and B modeled the output conductance and g_m is given by the total transconductance of M_1 and M_2 transistors, as follow:

$$C_D = C_{db2} + C_{gds1} + C_{gd4} + C_{db4} \quad (2)$$

$$C_X = C_{sb1} + C_{gs2} + C_{gd3} + C_{db3} \quad (3)$$

$$g_m = g_{m1}g_{m2} \quad (4)$$

$$A = g_{ds2} + g_{ds4} \quad (5)$$

$$B = g_{ds1} + g_{ds3} \quad (6)$$

The transistors of the AI were designed to obtain an inductance of around 7 nH at the frequency of 915 MHz.

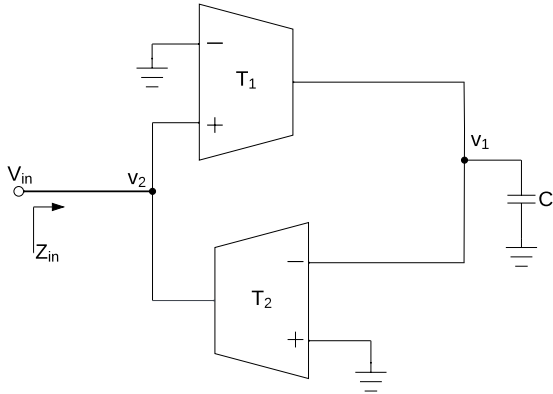


Fig. 2. Gyrator-C network.

TABLE I
DESIGN PARAMETERS USED IN THE AI IMPLEMENTATION IN A CMOS 65 NM TECHNOLOGY.

Transistor	L (μm)	W (μm)	Multipliers
M1	0.50	14.50	11
M2	0.50	14.50	9
M3	0.50	15.90	11
M4	0.50	20.35	18

For this design, the drain current flow through the branch of the $M1$ and $M3$ must be greater in relation to $M2$ and $M4$ branch [2]. Thus, to obtain the desired inductance it is needed a current drain (I_D) in $M1$ and $M3$ transistors of $550 \mu\text{A}$ and to other branch is needed a current of $442 \mu\text{A}$. For the implementation of the current sources, we have used channel length transistors higher than the minimum size to avoid the short channel effect on the output conductance.

Table I shows the transistor parameters used to obtain the target inductance value on the AI circuit.

The cadence virtuoso design environment $\text{\textcircled{R}}$ was used to simulate the circuit and to obtain the equivalent input impedance of the designed circuit. Fig. 5 shows the magnitude and phase of Z_{in} in the range from 100 MHz to 10 GHz. The inductor presents an inductance of 7.11 nH and a quality factor equal to Q of 14.44 at 915 MHz. The self-resonant frequency (SRF) of the proposed AI circuit occurs at 1.23 GHz.

Fig. 6 presents the generated inductance as a function of the frequency of the proposed AI circuit. The inductance value from 100 MHz to the SRF is in the range of 18.33 nH to 0 nH.

III. BANDPASS FILTER DESIGN

The tuned L-C network was used to design the proposed RF band-pass filter, shown in Fig. 7. It is composed of two reactive components (one inductor and one capacitor) in parallel connection [1] and a series resistor R .

The transfer function of the proposed active inductor-based BPF is given by Equation (7).

$$H(s) = \frac{s/(CR)}{s^2 + s/(CR) + 1/(LC)} \quad (7)$$

The filter center frequency (f_c) and quality factor (Q_f) can be evaluated as:

$$f_c = \frac{1}{2\pi\sqrt{LC}} \quad (8)$$

$$Q_f = 2\pi \cdot R \sqrt{\frac{C}{L}} = \frac{f_c}{BW} \quad (9)$$

in which the LC controls the resonance frequency and R adjusts the quality factor and bandwidth (BW).

Based on the value of the inductance obtained with the AI of $L = 7.11 \text{ nH}$ it is possible to obtain the required capacitor value to obtain the center frequency at 915 MHz using (10). It results in a capacitance of $C = 4.25 \text{ pF}$. The resistance must be $R = 200 \Omega$ to obtain a quality factor equal to $Q = 4.62$,

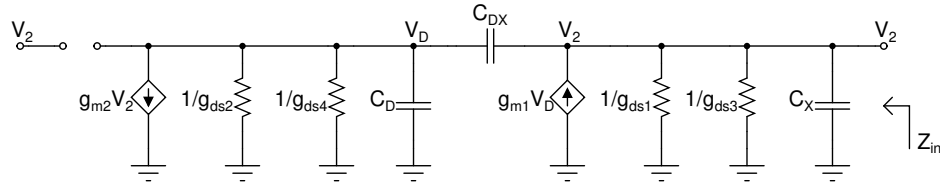


Fig. 3. Small-signal model of proposed AI circuit.

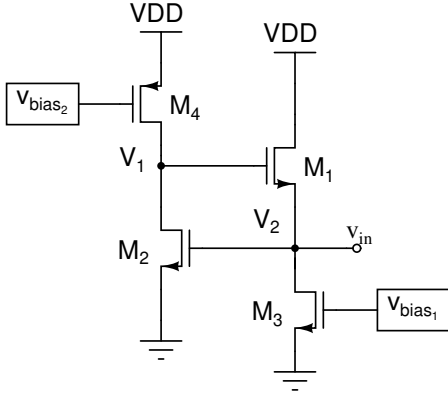


Fig. 4. Proposed active inductor topology.

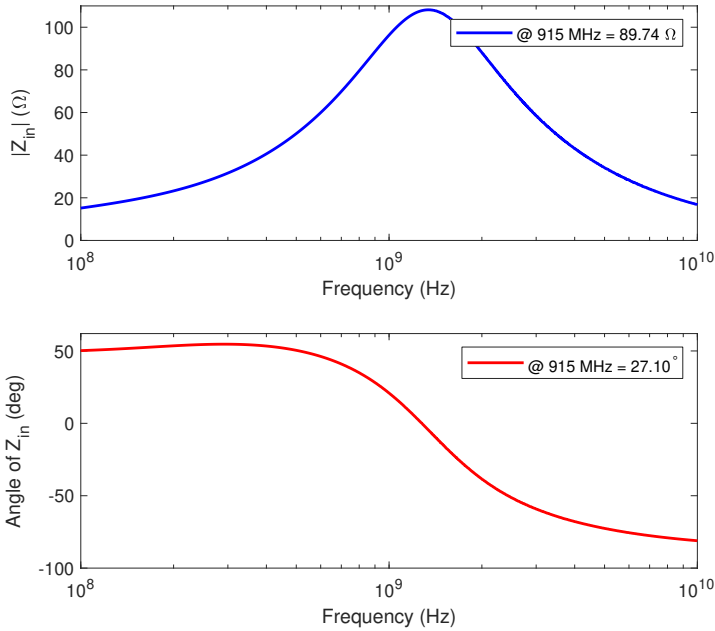


Fig. 5. Frequency response of equivalent impedance of proposed active inductor. Absolute value in blue and phase in red.

these parameters are given for the ideal circuit model of the proposed BPF. The ideal model of the proposed circuit reaches an attenuation equal to -2.52 dB and phase equal -0.74° at 915 MHz.

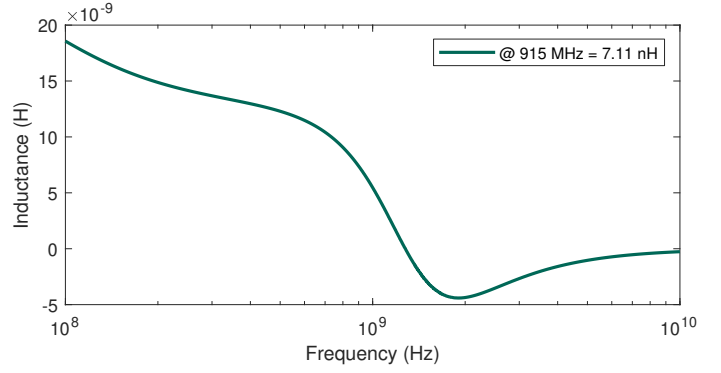


Fig. 6. Equivalent inductance generated by the proposed active inductor.

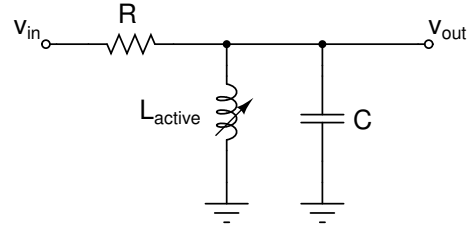


Fig. 7. Proposed bandpass filter.

$$C = \frac{1}{(2\pi f_0)^2 L_{active}} \quad (10)$$

However, the active inductor presents an equivalent parasitic parallel capacitance C_P and series resistances R_S , the Fig. 8 presents the RLC equivalent model of the proposed active inductor [4].

In this case, when the AI circuit is connected to the filter the own capacitance of the circuit makes a parallel connection with capacitance obtained from Equation (10), therefore it is needed to evaluate the value of C to compensate for the parasitic capacitance. After the compensation, the filter capacitance becomes equal to $C = 1$ pF. Consequently, the series resistance R_S also modifies the frequency response of the filter, thus the input resistance of the filter assumes the value equals $R = 390 \Omega$.

The proposed active inductor-based bandpass filter reaches 13.75 dB of insertion loss and phase equal -3.10° at 915 MHz, with a quality factor of $Q \approx 1.34$.

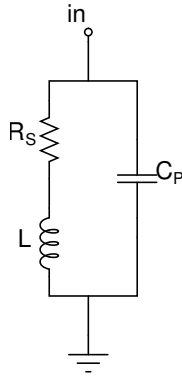


Fig. 8. Equivalent model of proposed AI.

Fig. 9 shows the frequency response of the proposed BPF employing the proposed active inductor and the ideal filter. As can be seen, both filters present the center frequency at 915 MHz as desired. However, due to the parasitic capacitor and resistance present in the AI, the obtained quality factor is lower and insertion loss is higher in comparison to the ideal circuit.

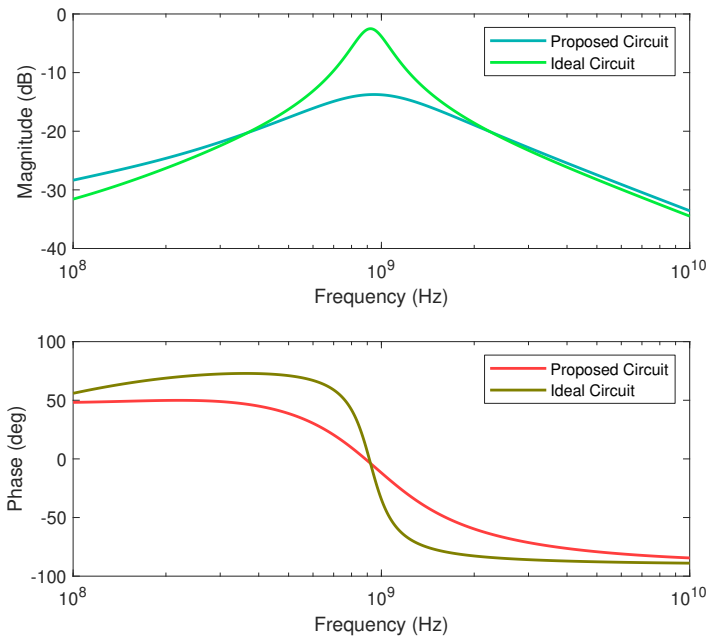


Fig. 9. Frequency response of proposed band-pass filter and the ideal filter.

IV. CONCLUSION

This paper has presented the preliminary results of an active inductor-based bandpass filter implemented in a 65nm CMOS process. The designed active inductor (AI) presented an inductance of 7.11 nH with Q of 14.44 at 915 MHz and SRF equal to 1.23 GHz. The AI was used to implement a bandpass filter at a frequency of 915 MHz. This filter presented 13.75 dB of insertion loss with a Q of 1.34, which represents a bandwidth of 680 MHz.

In future works, we intend to improve the AI implementation to reduce its parasitic elements, improve its quality factor, and reduce power consumption. Additionally we intend to implement other topologies of filter using the design AI.

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